PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2001-223288
(43)Date of publication of application : 17.08.2001

(51)Int.Cl. H01L 23/12
H01L 21/301

(21)Application number : 2000-029236
(22)Date of filing : 07.02.2000

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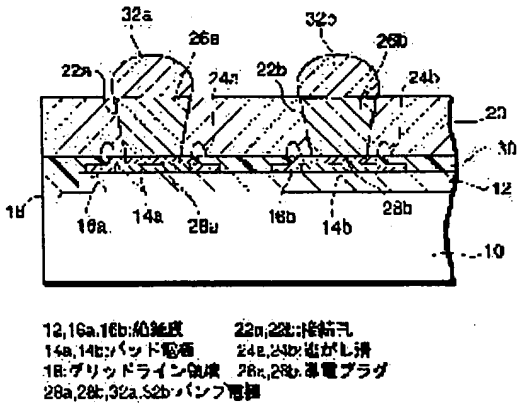
(54) INTEGRATED CIRCUIT DEVICE AND ITS MANUFACTURING METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To reduce the package size of an IC (integrated circuit) having a chip size package.
SOLUTION: A pad electrode 14a being connected with an IC is formed on an insulation film 12 covering the surface of the IC chip region of a semiconductor wafer. A contact hole 22a made in the chip region for protecting the IC chip region of a glass protection board is filled with a conduction plug 26a and a relief groove 24a surrounding the contact hole 22a, a bump electrode 28a connected with the plug 26a, and an adhesion layer 30 of thermoplastic adhesive are provided on the lower surface side. When the electrode 28a is connected with the electrode 14a, the IC is sealed by bonding the wafer and the protection board through the adhesion layer 30 and a bump electrode 32a is formed on the plug 26a. Finally, an IC device comprising an IC chip 10 and a protection chip 20 is separated, by dicing, from a laminate of the wafer and the protection board.



12,16a,16b:絶縁膜 22a,22b:接続孔
14a,14b:パッド電極 24a,24b:逃がし溝
18:グリッドライン領域 26a,26b:導電プラグ
28a,28b,32a,32b:バンプ電極

LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]